**1. What is the primary focus of Transaction Level Modeling (TLM)?**

* A) Signal-level toggling
* B) Gate-level simulation
* C) Data transfers between modules
* D) Power estimation  
  **Answer:** C

**2. TLM models are typically implemented using which language/library?**

* A) Verilog
* B) SystemC
* C) VHDL
* D) C  
  **Answer:** B

**3. In TLM, a transaction is best described as:**

* A) A signal
* B) A class object containing communication data
* C) A register
* D) A clock cycle  
  **Answer:** B

**4. Which version of TLM introduced the concept of unified sockets?**

* A) TLM 1.0
* B) TLM 2.0
* C) TLM 2.0.1
* D) TLM 0.9  
  **Answer:** B

**5. What is a major advantage of TLM over RTL modeling?**

* A) More accurate timing
* B) Faster simulation speed
* C) Lower abstraction
* D) More detailed signal tracing  
  **Answer:** B

**6. In TLM, which mechanism is commonly used to buffer transactions?**

* A) Register
* B) FIFO
* C) Latch
* D) Multiplexer  
  **Answer:** B

**7. Which of the following is NOT a typical TLM communication style?**

* A) Unidirectional
* B) Bidirectional
* C) Broadcasting
* D) Synchronous reset  
  **Answer:** D

**8. What does TLM abstract away in a digital system?**

* A) Data
* B) Low-level signal details
* C) Functional units
* D) Software  
  **Answer:** B

**9. Which of the following is a key feature of TLM 2.0?**

* A) Only get/put interfaces
* B) Generic payload class
* C) No support for sockets
* D) Only SystemVerilog support  
  **Answer:** B

**10. What is the main purpose of using ports and exports in TLM?**

* A) To create clock domains
* B) To connect and communicate between components
* C) To synthesize hardware
* D) To define memory size  
  **Answer:** B

**11. Which TLM communication mode allows the sender to continue execution without waiting?**

* A) Blocking
* B) Nonblocking
* C) Synchronous
* D) Asynchronous reset  
  **Answer:** B

**12. In UVM, transactions are derived from which base class?**

* A) uvm\_component
* B) uvm\_transaction
* C) uvm\_object
* D) uvm\_sequence  
  **Answer:** B

**13. Which of the following is NOT a benefit of TLM?**

* A) Reusable in different environments
* B) Plug and play connections
* C) Requires detailed signal-level design
* D) Hides unnecessary internal details  
  **Answer:** C

**14. Which abstraction level is higher: TLM or RTL?**

* A) TLM
* B) RTL
* C) Both are same
* D) It depends  
  **Answer:** A

**15. What is the role of sockets in TLM 2.0?**

* A) Provide power estimation
* B) Unify initiator/target connections
* C) Generate clock signals
* D) Handle reset logic  
  **Answer:** B

**16. Which TLM version introduced the generic payload?**

* A) TLM 1.0
* B) TLM 2.0
* C) TLM 2.0.1
* D) TLM 0.9  
  **Answer:** B

**17. What does a TLM channel typically model?**

* A) Data path
* B) Control path
* C) Communication medium like a bus or FIFO
* D) Power supply  
  **Answer:** C

**18. Which of the following is NOT a TLM port type?**

* A) Analysis port
* B) Export
* C) Imp port
* D) Flip-flop port  
  **Answer:** D

**19. What is the main use of TLM in SoC design?**

* A) Gate-level simulation
* B) System-level analysis and verification
* C) Power analysis
* D) Synthesis  
  **Answer:** B

**20. In TLM, what does "blocking" communication mean?**

* A) Sender waits for transaction completion
* B) Sender never waits
* C) Only used for resets
* D) Only used for clocks  
  **Answer:** A

**21. TLM enables which kind of connections between components?**

* A) Only one-to-one
* B) One-to-many and many-to-one
* C) Only one-to-many
* D) Only many-to-many  
  **Answer:** B

**22. Which of the following is NOT an advantage of TLM?**

* A) Faster simulation
* B) Simplified testbench
* C) Increased signal-level detail
* D) Easy component replacement  
  **Answer:** C

**23. What is the primary modeling approach in TLM?**

* A) Signal-level modeling
* B) Transaction-based modeling
* C) Gate-level modeling
* D) Behavioral modeling only  
  **Answer:** B

**24. Which of the following is a valid TLM communication pattern?**

* A) Producer-consumer
* B) Consumer-producer only
* C) Clock-synchronous only
* D) Power-aware only  
  **Answer:** A

**25. What is the main benefit of using TLM in early design stages?**

* A) Accurate gate-level delays
* B) Early software development and integration
* C) Power estimation
* D) Synthesis  
  **Answer:** B

**26. Which of the following is true about TLM ports and exports?**

* A) They must be interface compatible
* B) They can be connected arbitrarily
* C) Only ports are needed
* D) Only exports are needed  
  **Answer:** A

**27. Which abstraction level comes after TLM in the design hierarchy?**

* A) Algorithmic level
* B) RTL
* C) Gate level
* D) Behavioral level  
  **Answer:** B

**28. What is the main difference between TLM 1.0 and TLM 2.0?**

* A) TLM 2.0 supports unified sockets and generic payload
* B) TLM 1.0 supports sockets
* C) TLM 1.0 supports generic payload
* D) No difference  
  **Answer:** A

**29. Which of the following is NOT a typical use of TLM?**

* A) System architecture exploration
* B) Early software development
* C) Power grid analysis
* D) HW/SW co-design  
  **Answer:** C

**30. What is a peer-to-peer connection in TLM?**

* A) Connection through multiple routers
* B) Direct connection between two components
* C) Connection via clock domain crossing
* D) Only through analysis ports  
  **Answer:** B